# PCM-DRAM Hybrid Memory – Next Generation Storage

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## Phase Change Memory (PCM)
- Non-volatile storage devices
- Use electrical signals to change crystal structure from crystalline to amorphous and vise versa

## A Promising Candidate to Replace DRAM!
- **Higher Density**: PCM has a smaller feature size than DRAM
- **Low Power**: PCM is non-volatile, while DRAM is volatile and needs to continuously refresh storage capacitors.

## PCM vs. DRAM
<table>
<thead>
<tr>
<th></th>
<th>DRAM</th>
<th>PCM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Size</strong></td>
<td>68 nm</td>
<td>65 nm</td>
</tr>
<tr>
<td><strong>Write Speed</strong></td>
<td>10 ns</td>
<td>50 ns</td>
</tr>
<tr>
<td><strong>Read Speed</strong></td>
<td>10 ns</td>
<td>60 ns</td>
</tr>
<tr>
<td><strong>Retention</strong></td>
<td>64 ms</td>
<td>10 years</td>
</tr>
<tr>
<td><strong>Endurance</strong></td>
<td>3E+16</td>
<td>1E+8</td>
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</tbody>
</table>

## Two Critical Problems To Solve!
- **Slower**: Each read and write takes longer time
- **Limited Endurance**: Each PCM cell can only be written for limited times

## Endurance Enhancement:
- Use DRAM buffer to absorb most of memory writes
- Bring data directly to DRAM upon page faults.
- Modify clock algorithm to map hot virtual pages to cold physical pages and vise versa.
- Use wear leveling techniques to evenly distribute the writes to PCM cells.

## Read/Write Acceleration:
- Access the DRAM buffer for most reads and writes.
- 4MB DRAM is sufficient to bridge most of the latency gap of a 1GB PCM.